

DECLARATION

As the below-named inventors, we declare that:

Our residences, post office addresses, and citizenships are as stated below under our names.


We believe we are the original, first, and joint inventors of the invention entitled "SEMICONDUCTOR PACKAGE ASSEMBLY AND METHOD FOR ELECTRICALLY ISOLATING MODULES," which is described and claimed in the foregoing application and for which a patent is sought. This application claims the benefit of earlier filed United Kingdom Patent Application No. 0126821.8, filed on November 7, 2001.

We have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referred to herein (if any).

We acknowledge our duty to disclose information of which we are aware which is material to patentability and examination of this application in accordance with 37 C.F.R. § 1.56(a).

We further declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that the making of willfully false statements and the like is punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and may jeopardize the validity of any patent issuing from this patent application.

Applicants' counsel is authorized to insert the official filing date and application number information when it becomes available.


Sion C. Quinlan

Date

02 January 2002

Residence

:

City of Goring on Thames, Oxon

United Kingdom

Citizenship

:

British

P.O. Address

:

1, Lockstile Way

Goring on Thames, Oxon RG8

United Kingdom


Tim J. Bales

Date

02nd January 2002

Residence

:

City of Bracknell, England

United Kingdom

Citizenship

:

British

P.O. Address

:

15 Derbyshire Green, Warfield

Bracknell, England

United Kingdom

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Sion C. Quinlan and Tim J. Bales Attorney Docket No.: 500986.02
Filed : Concurrently herewith
Title : SEMICONDUCTOR PACKAGE ASSEMBLY AND METHOD FOR ELECTRICALLY
ISOLATING MODULES

Box Patent Application
Commissioner of Patents
Washington, DC 20231

ELECTION UNDER 37 C.F.R. §§ 3.71 AND 3.73(b) AND POWER OF ATTORNEY

Sir:

The undersigned, being Assignee of the entire interest in the above-identified application by virtue of an Assignment filed concurrently herewith, hereby elects, under 37 C.F.R. § 3.71, to prosecute the application to the exclusion of the inventors.

Assignee hereby appoints EDWARD W. BULCHIS, Reg. No. 26,847; PAUL T. MEIKLEJOHN, Reg. No. 26,569; GLENN P. RICKARDS, Reg. No. 29,428; DALE C. BARR, Reg. No. 40,498; KIMTON N. ENG, Reg. No. 43,605; BRIAN C. PARK, Reg. No. 45,519; MARK W. ROBERTS, Reg. No. 46,160; STEVEN H. ARTERBERRY, Reg. No. 46,314; PAUL F. RUSYN, Reg. No. 42,118; ANDREW F. PRATT, Reg. No. 48,985; FRANK J. BOZZO, Reg. No. 36,756; JAMES ACKLEY, Reg. No. 45,695; RONALD BROWN, Reg. No. 29,016; DAVID BRUHN, Reg. No. 36,762; MARK CARLSON, Reg. No. 27,105; KEVIN CHAPPLE, Reg. No. 44,072; W. ROBINSON CLARK, Reg. No. 41,530; SHANE COLEMAN, Reg. No. 44,623; GREGORY DURBIN, Reg. No. 42,503; DANIEL FISHER, Reg. No. 34,162; DAVID FRONEK, Reg. No. 25,678; ANTHONY GANGEMI, Reg. No. 42,565; MICHAEL GILCHRIST, Reg. No. 40,619; THERESA HANKES, Reg. No. 45,501; JOHN HARROP, Reg. No. 41,817; BRAD HATTENBACH, Reg. No. 42,642; REED HEIMBECHER, Reg. No. 36,353; CRAIG HEMENWAY, Reg. No. 44,759; STUART HEMPHILL, Reg. No. 28,084; MARK HOGGE, Reg.

No. 31,622; JOHN KENNEDY, Reg. No. 42,717; JASON KRAUS, Reg. No. 42,765; BRIAN LAURENZO, Reg. No. 34,207; KENNETH LEVITT, Reg. No. 39,747; KURT LEYENDECKER, Reg. No. 42,799; SCOTT MARKS, Reg. No. 44,902; KEITH MONTGOMERY, Reg. No. 45,245; ALDO NOTO, Reg. No. 35,628; LEE OSMAN, Reg. No. 38,260; DEVAN PADMANABHAN, Reg. No. 38,262; JAMES PINTO, Reg. No. 40,774; GARY POLUMBUS, Reg. No. 25,364; SCOTT ROTHENBERGER, Reg. No. 41,277; LEONARD SANTISI, Reg. No. 24,135; ROBERT SCHEFFEL, Reg. No. 43,090; AMI SHAH, Reg. No. 41,143; MIRIAM SOHN, Reg. No. 35,368; HERMES SOYEZ, Reg. No. 45,852; GERALD SULLIVAN, Reg. No. 37,243; MARK THOMAS, Reg. No. 37,953; JON TUTTLE, Reg. No. 25,713; MEGAN VALENTINE, Reg. No. 47,149; LANCE VIETZKE, Reg. No. 36,708; SEAN WOODEN, Reg. No. 43,997; and the attorneys and agents associated with the firm of **DORSEY & WHITNEY LLP, Customer Number 27,076**, along with MICHAEL L. LYNCH, Reg. No. 30,871; CHARLES B. BRANTLEY, II, Reg. No. 38,086; KEVIN D. MARTIN, Reg. No. 37,882; and DAVID J. PAUL, Reg. No. 34,692, of MICRON TECHNOLOGY, INC., 8000 South Federal Way, Boise, Idaho 83716-9632, as its attorneys to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. Please direct all telephone calls to **Andrew F. Pratt** at (206) 903-8800 and telecopies to (206) 903-8820.


Please direct all communications to:

Andrew F. Pratt, Esq.
Customer No. 27,076
Dorsey & Whitney LLP
1420 Fifth Avenue, Suite 3400
Seattle, Washington 98101
(206) 903-8800

Pursuant to 37 C.F.R. § 3.73(b), the undersigned duly authorized designee of Assignee certifies that the evidentiary documents have been reviewed, specifically the Assignment to MICRON TECHNOLOGY, INC., filed concurrently herewith for recording, a copy of which is attached hereto, and certifies that to the best of my knowledge and belief, title remains in the name of the Assignee.

MICRON TECHNOLOGY, INC.
ASSIGNEE

1-14-2002
DATE


Michael L. Lynch
Chief Patent Counsel

Enclosure:
Copy of Assignment

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Sion C. Quinlan and Tim J. Bales

Filed : Concurrently herewith

For : SEMICONDUCTOR PACKAGE
ASSEMBLY AND METHOD FOR
ELECTRICALLY ISOLATING
MODULES

Docket No. 500986.02

Disclosure No. 00-0762.01

ASSIGNMENT :

 X Enclosed for recording

 Previously recorded

Date: _____

Reel: _____

FOR GOOD AND VALUABLE CONSIDERATION, the receipt, sufficiency and adequacy of which are hereby acknowledged, the undersigned do hereby:

SELL, ASSIGN AND TRANSFER to **Micron Technology, Inc.** (the "Assignee"), a corporation of Delaware, having a place of business at 8000 South Federal Way, Boise, Idaho 83716-9632, the entire right, title and interest for the United States and all foreign countries, in and to any and all improvements which are disclosed in the application for United States Letters Patent, which has been executed by the undersigned concurrently herewith and is entitled "**SEMICONDUCTOR PACKAGE ASSEMBLY AND METHOD FOR ELECTRICALLY ISOLATING MODULES**"; such application and all divisional, continuing, substitute, renewal, reissue and all other applications for patent which have been or shall be filed in the United States and all foreign countries on any of such improvements; all original and reissued patents which have been or shall be issued in the United States and all foreign countries on such improvements; and specifically including the right to file foreign applications under the provisions of any convention or treaty and claim priority based on such application in the United States of America. This application claims the benefit of earlier filed United Kingdom Patent Application No. 0126821.8, filed November 7, 2001;

AUTHORIZE AND REQUEST the issuing authority to issue any and all United States and foreign patents granted on such improvements to the Assignee;

WARRANT AND COVENANT that no assignment, grant, mortgage, license or other agreement affecting the rights and property herein conveyed has been or will be made to others by the undersigned, and that the full right to convey the same as herein expressed is possessed by the undersigned;

COVENANT that, when requested and at the expense of the Assignee, to carry out in good faith the intent and purpose of this assignment, the undersigned will execute all divisional, continuing, substitute, renewal, reissue, and all other patent applications on any and all such improvements; execute all rightful oaths, declarations, assignments, powers of attorney and other papers; communicate to the Assignee all facts known to the undersigned relating to such improvements and the history thereof; and generally do everything possible which the Assignee shall consider desirable for securing, maintaining and enforcing proper patent protection for such improvements and for vesting title to such improvements in the Assignee;

TO BE BINDING on the heirs, assigns, representatives and successors of the undersigned and extend to the successors, assigns and nominees of the Assignee.

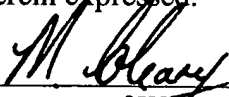
APPLICANTS' counsel is authorized to insert the official filing date and application number information when it becomes available.



Sion C. Quinlan

Date: 2 January 2002 .

BEFORE ME, this 2nd day of January, 2002, personally appeared the above-named individual, to me known to be the person who is described in and who executed the foregoing assignment instrument and acknowledged to me that he/she executed the same of his/her own free will for the purpose therein expressed.



Signature of Witness

X Bales
Tim J. Bales

Date: 02nd January 2002

BEFORE ME, this 2nd day of January, 2002, personally appeared the above-named individual, to me known to be the person who is described in and who executed the foregoing assignment instrument and acknowledged to me that he/she executed the same of his/her own free will for the purpose therein expressed.

M. Bales
Signature of Witness

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